

FIG. 1  
(PRIOR ART)

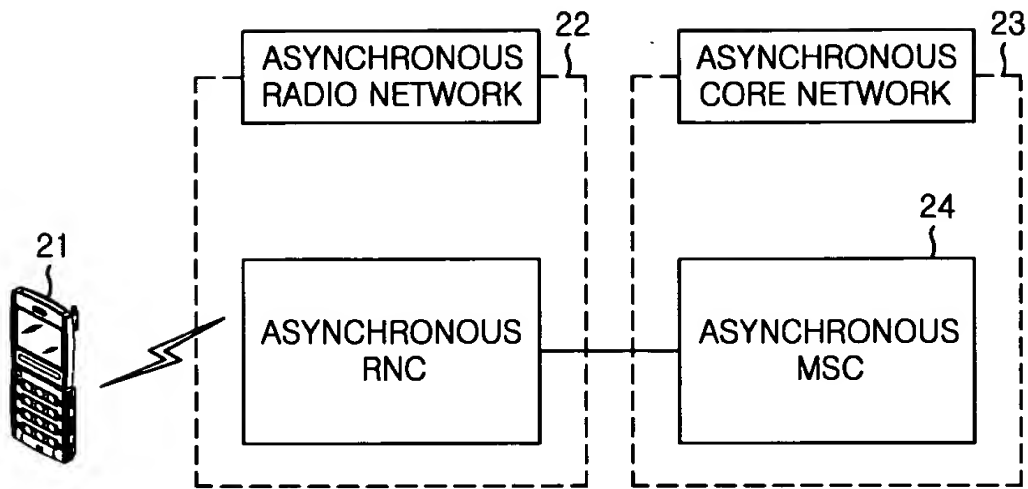


FIG. 2  
(PRIOR ART)

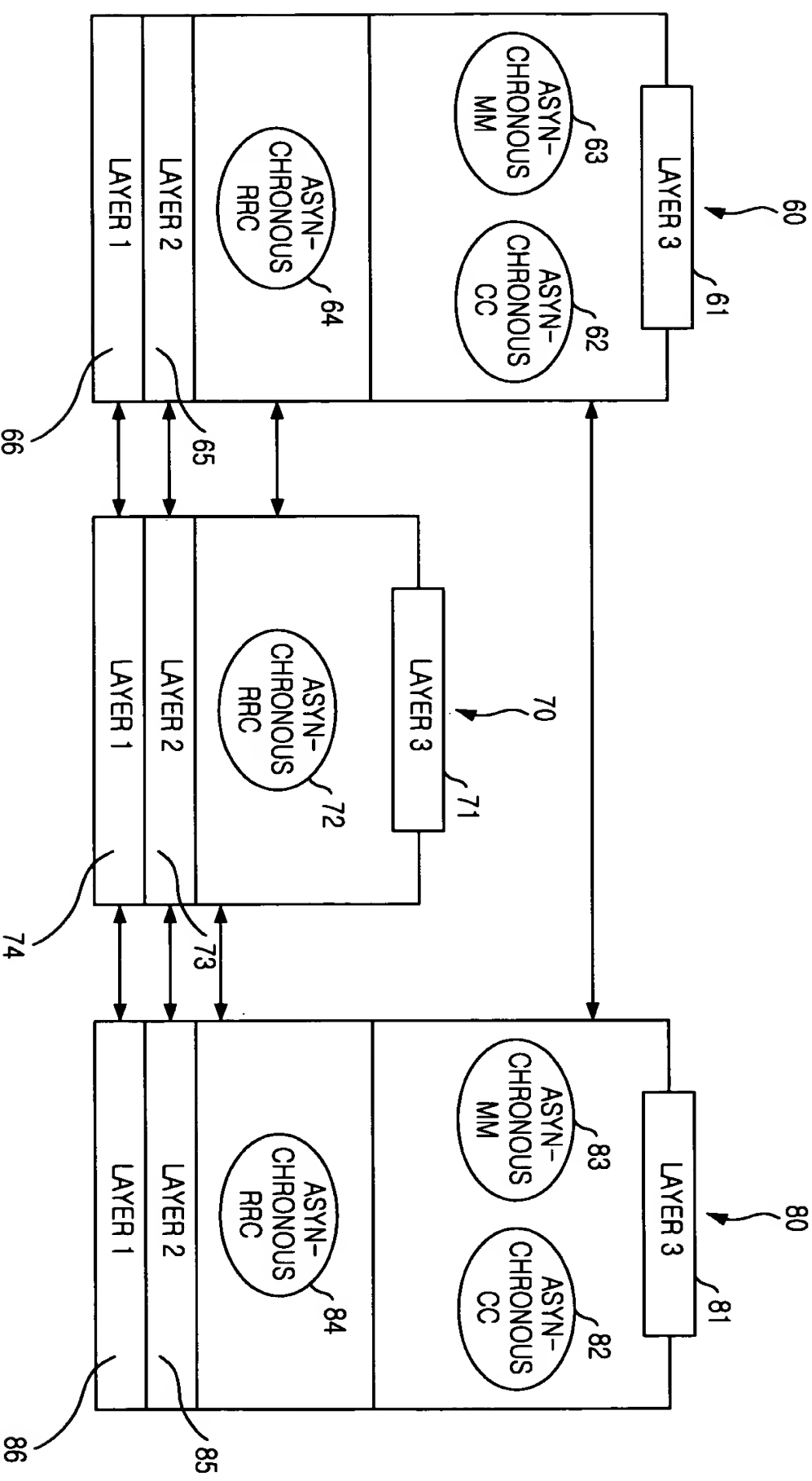


FIG. 3A

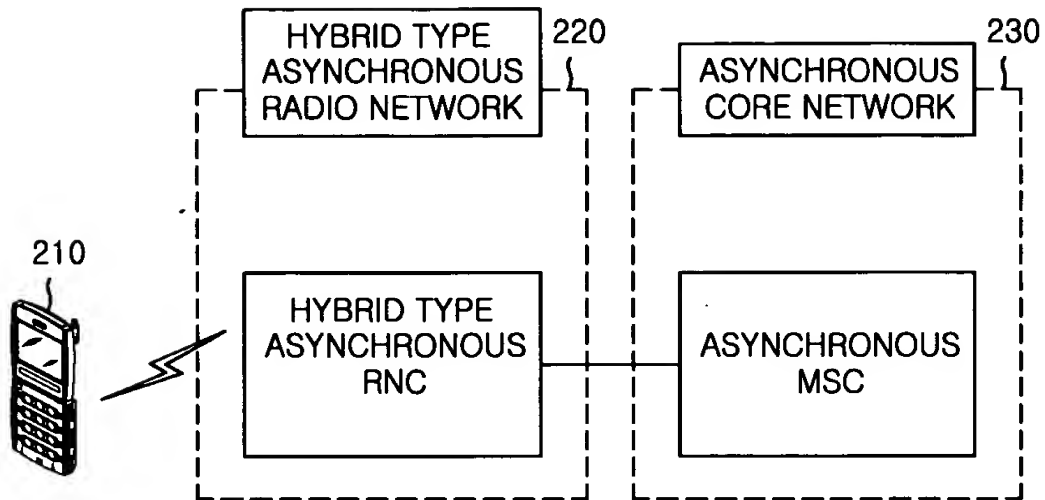


FIG. 3B

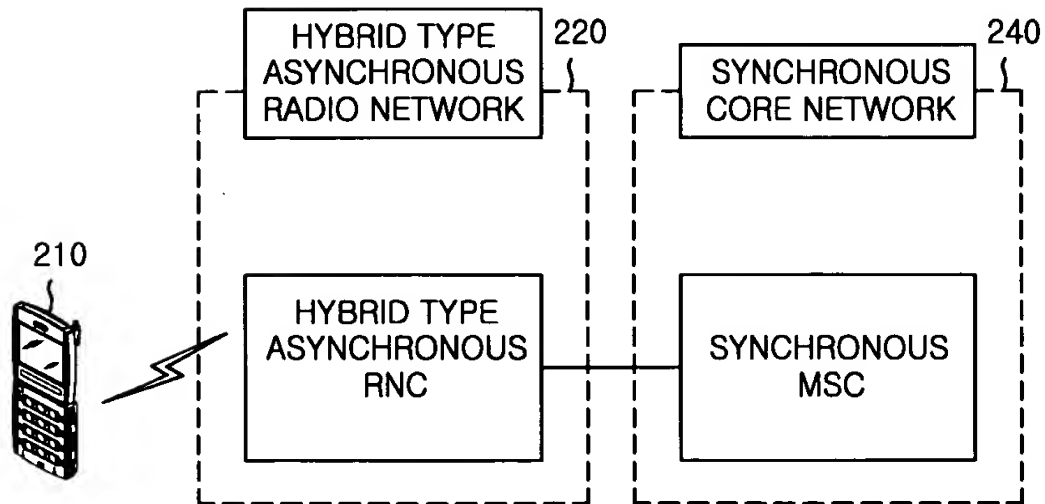


Figure 1 illustrates a system architecture with three parallel processing paths, labeled 210, 220, and 230. Each path is composed of three main layers: LAYER 3, LAYER 2, and LAYER 1.

- Path 210:** LAYER 3 (211) contains two components: ASYN-CHRONOUS MM (215) and SYN-CHRONOUS MM (213). LAYER 2 (217) contains two components: ASYN-CHRONOUS RRC (216) and SYN-CHRONOUS CC (212). LAYER 1 (218) contains two components: ASYN-CHRONOUS RRC (216) and SYN-CHRONOUS CC (212).
- Path 220:** LAYER 3 (221) contains two components: ASYN-CHRONOUS MM (223) and SYN-CHRONOUS MM (222). LAYER 2 (225) contains two components: ASYN-CHRONOUS RRC (224) and SYN-CHRONOUS CC (222). LAYER 1 (226) contains two components: ASYN-CHRONOUS RRC (224) and SYN-CHRONOUS CC (222).
- Path 230:** LAYER 3 (231) contains two components: ASYN-CHRONOUS MM (233) and SYN-CHRONOUS MM (232). LAYER 2 (235) contains two components: ASYN-CHRONOUS RRC (234) and SYN-CHRONOUS CC (232). LAYER 1 (236) contains two components: ASYN-CHRONOUS RRC (234) and SYN-CHRONOUS RR (234).

Arrows indicate the flow of data and control signals between the components within each layer and between the layers themselves. Specifically, arrows show connections between LAYER 3 and LAYER 2, and between LAYER 2 and LAYER 1, as well as direct connections between LAYER 3 and LAYER 1.

FIG. 4B

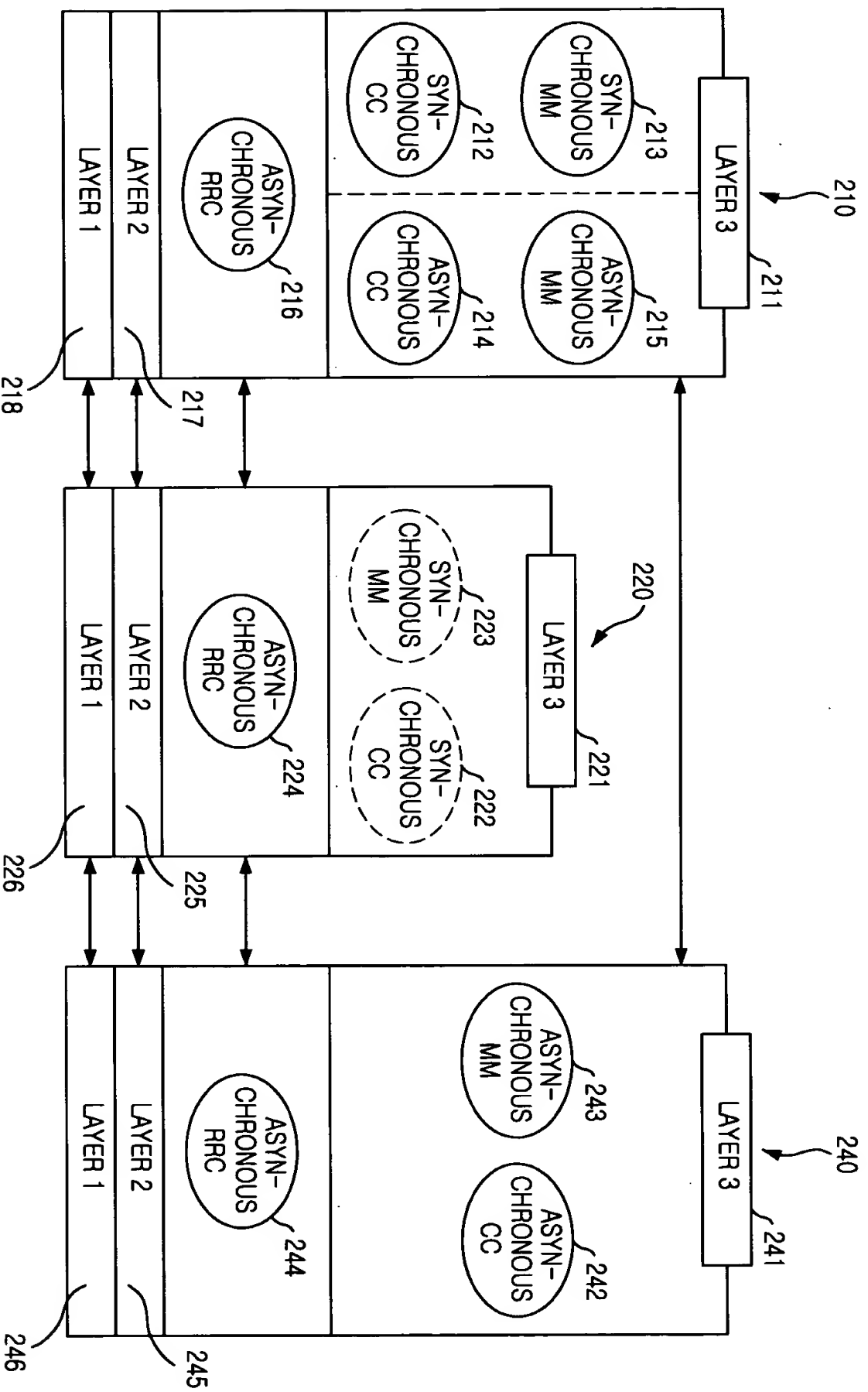


FIG. 5A

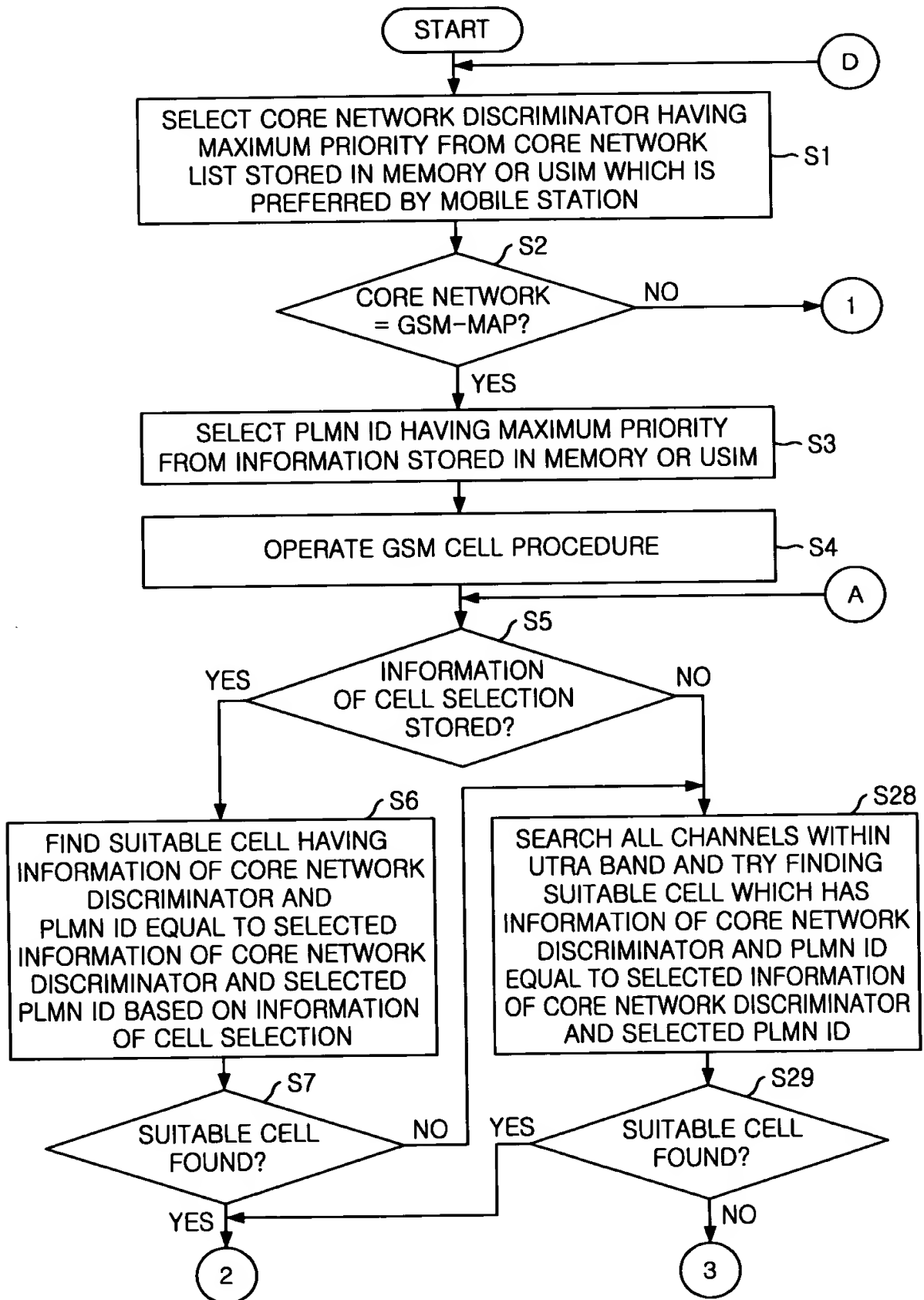


FIG. 5B

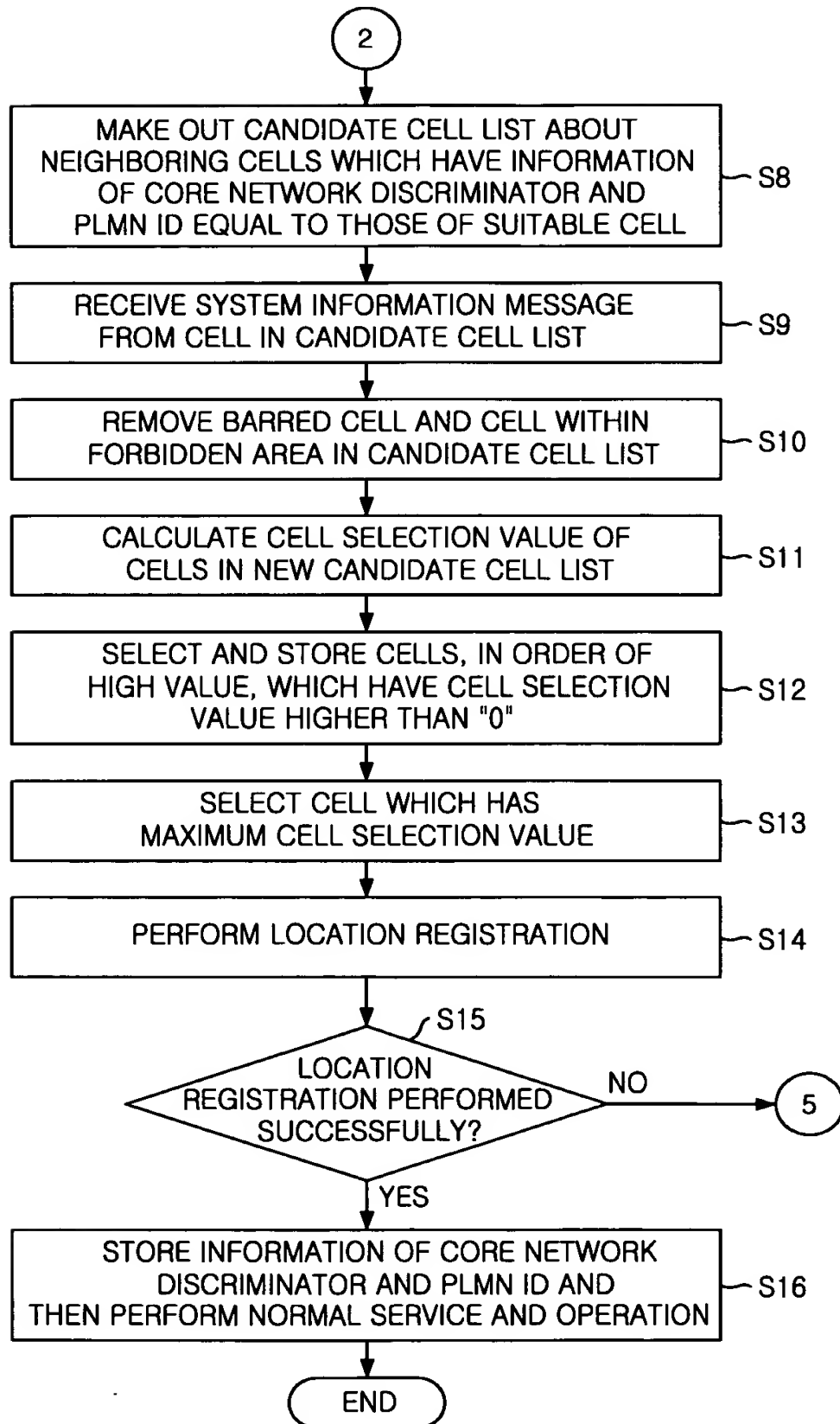


FIG. 5C

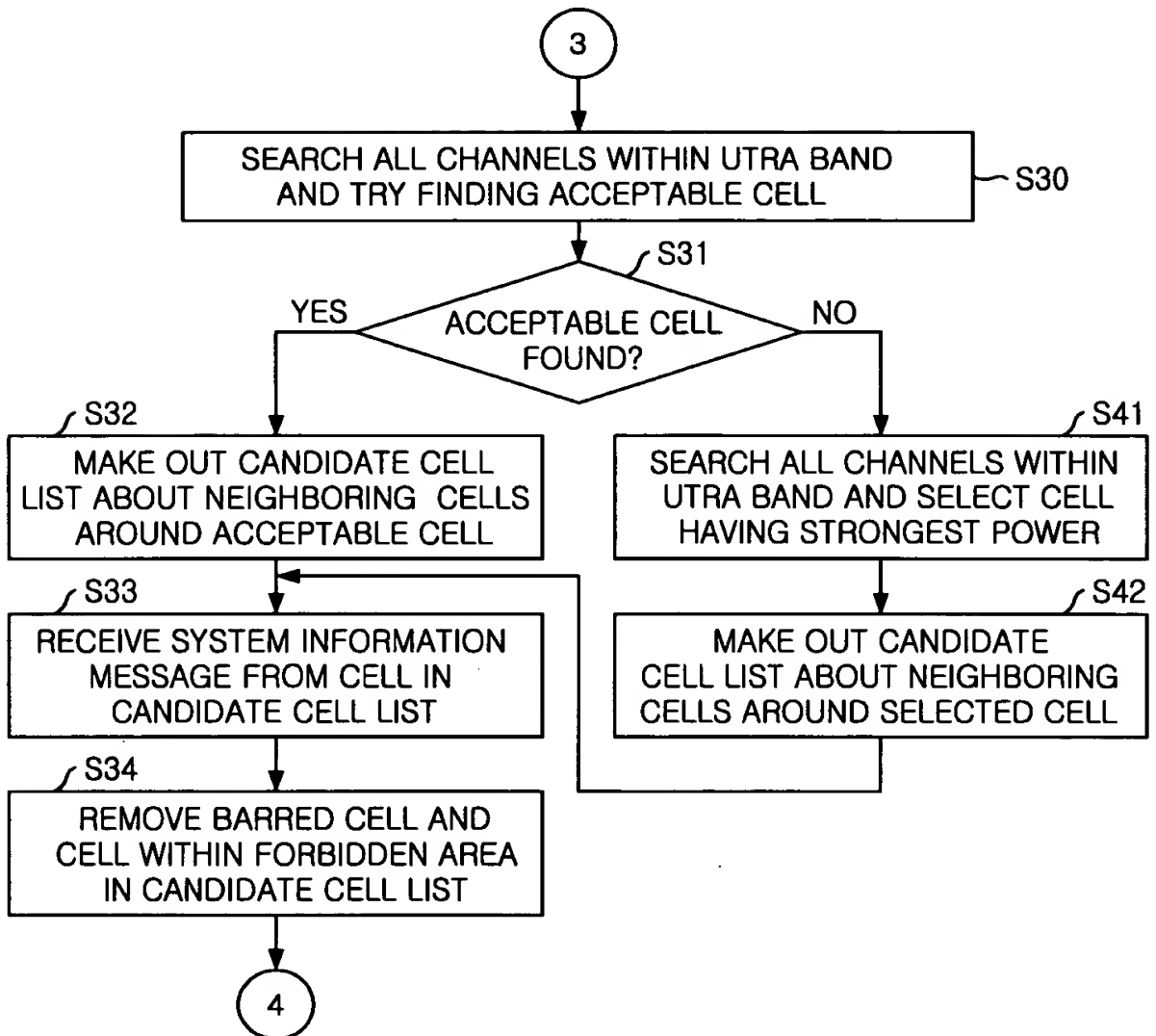




FIG. 5D

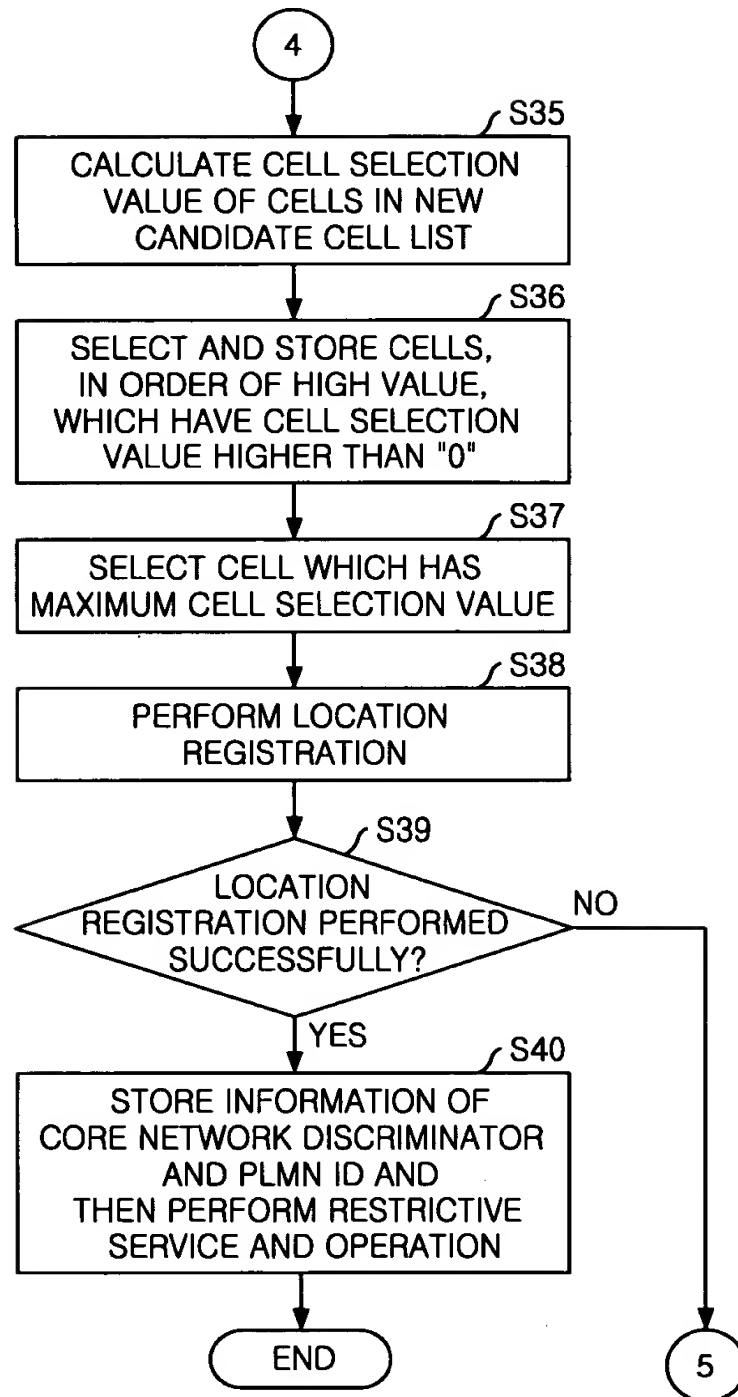


FIG. 5E

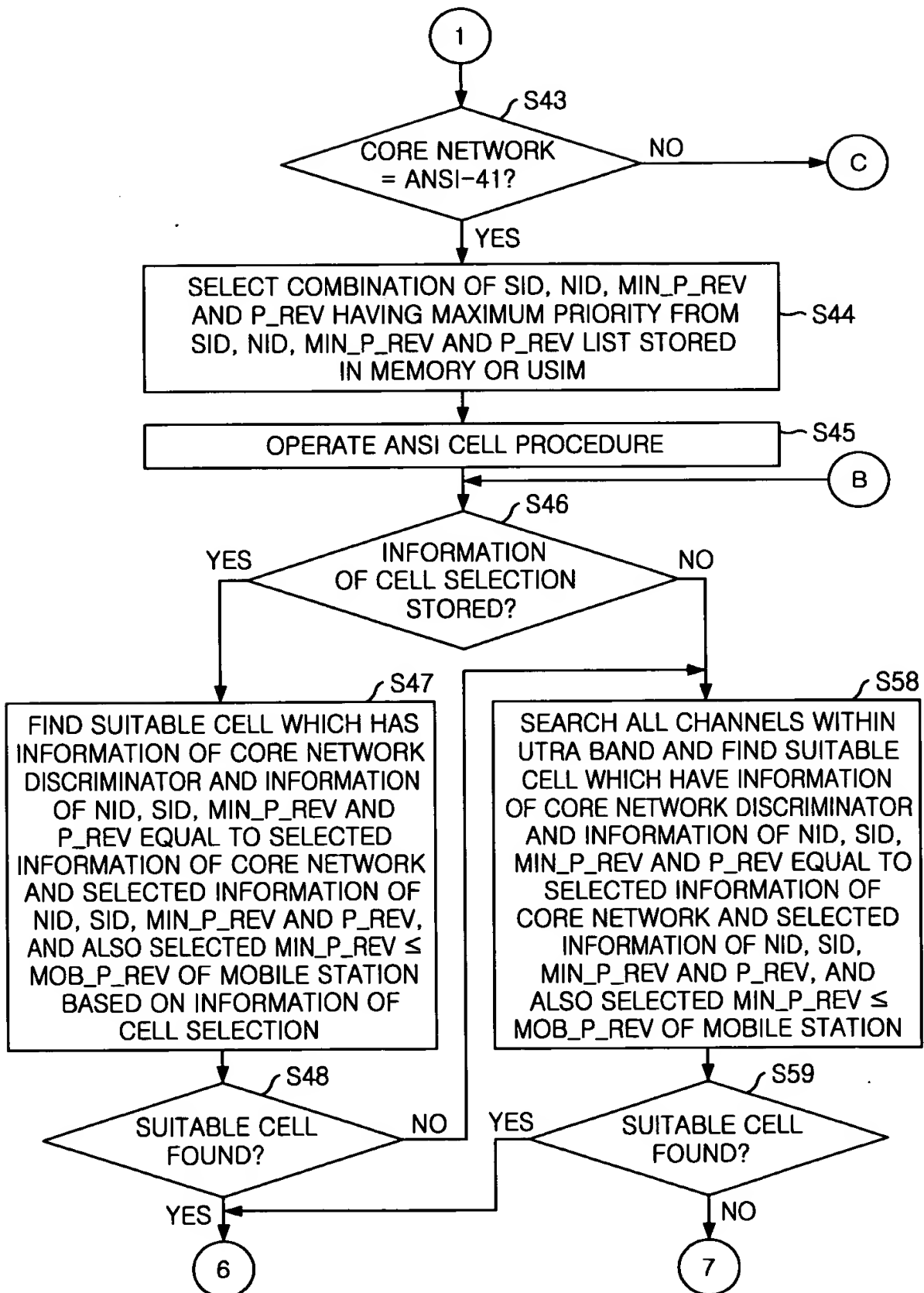


FIG. 5F

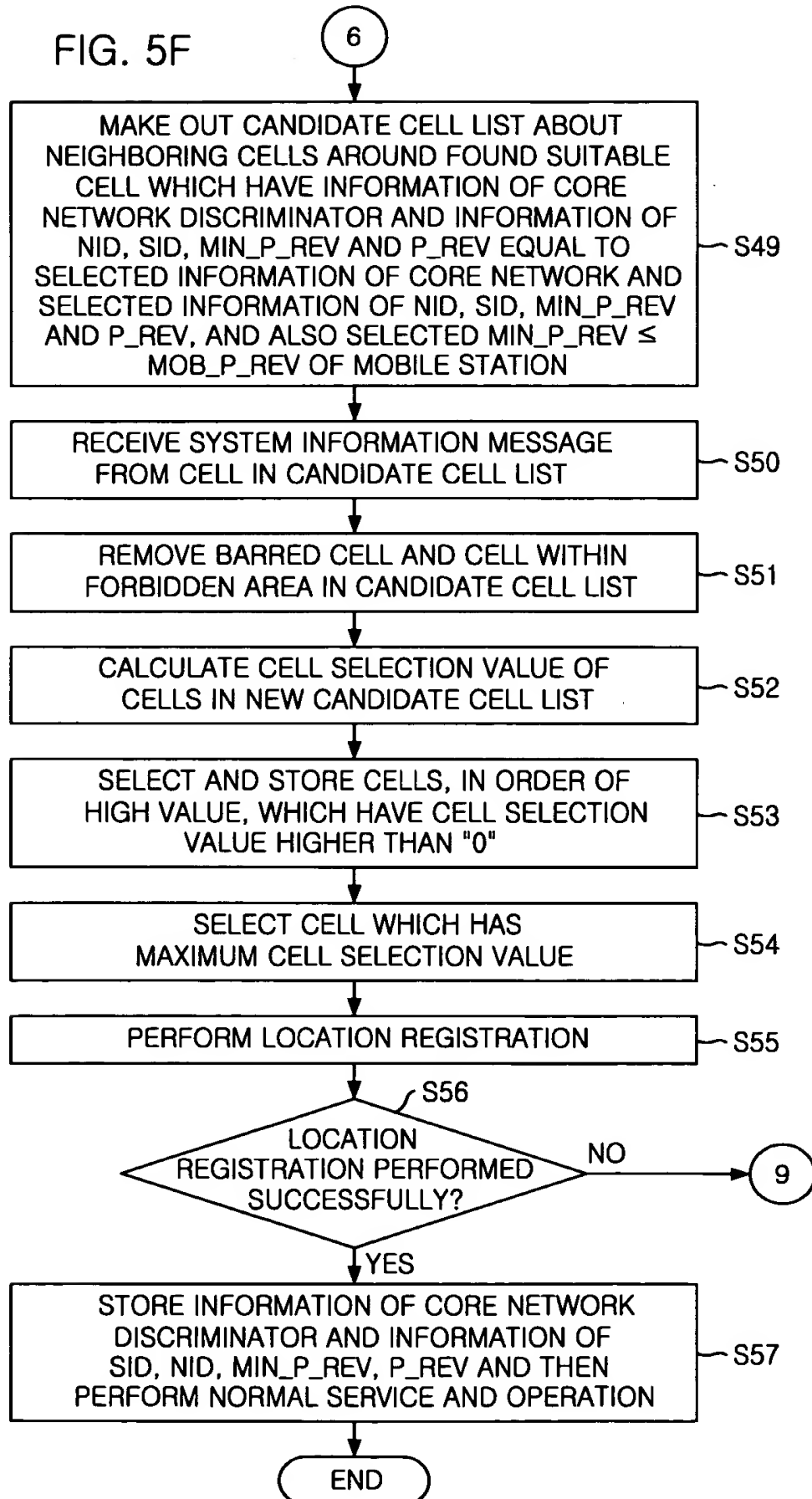


FIG. 5G

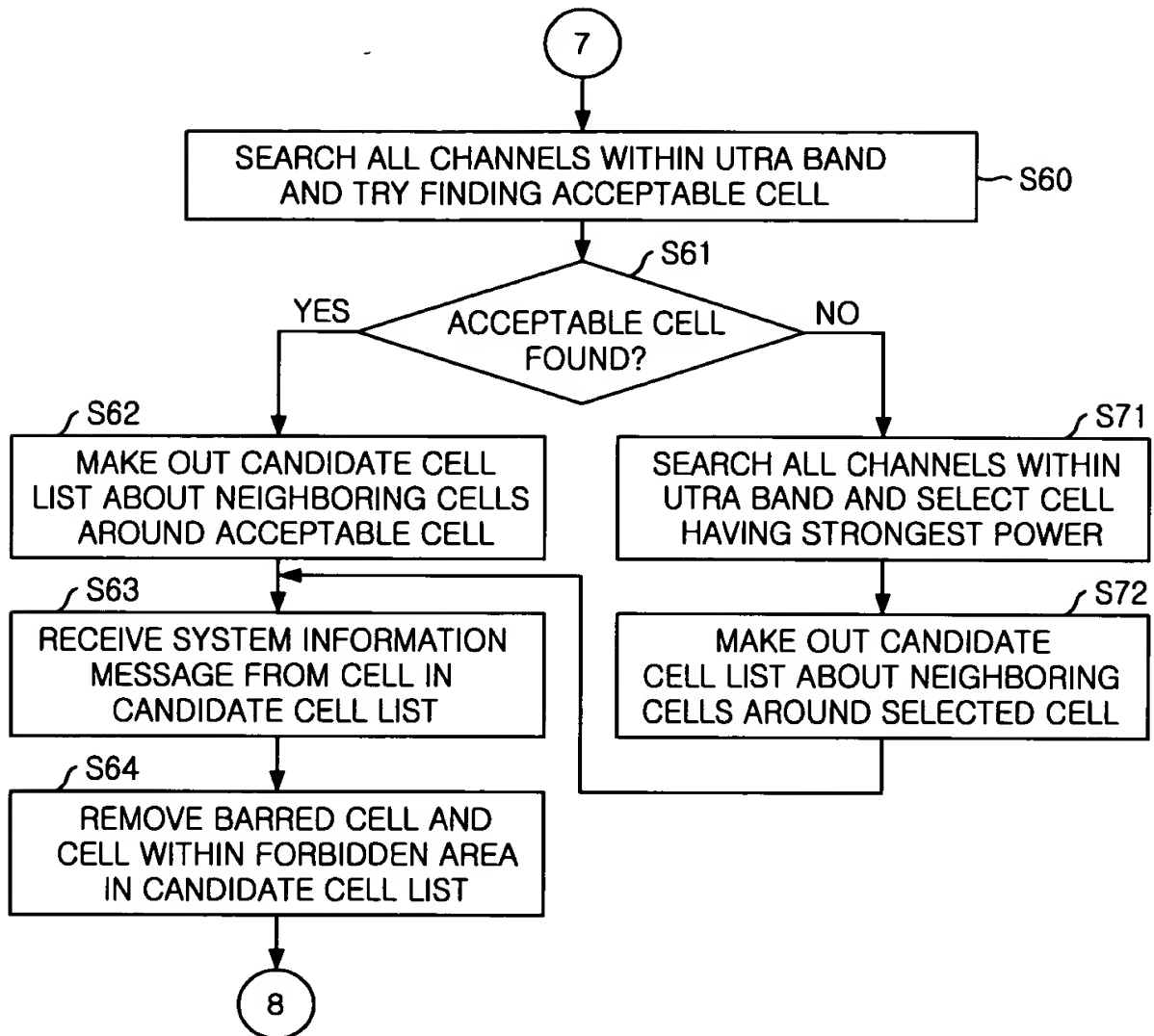
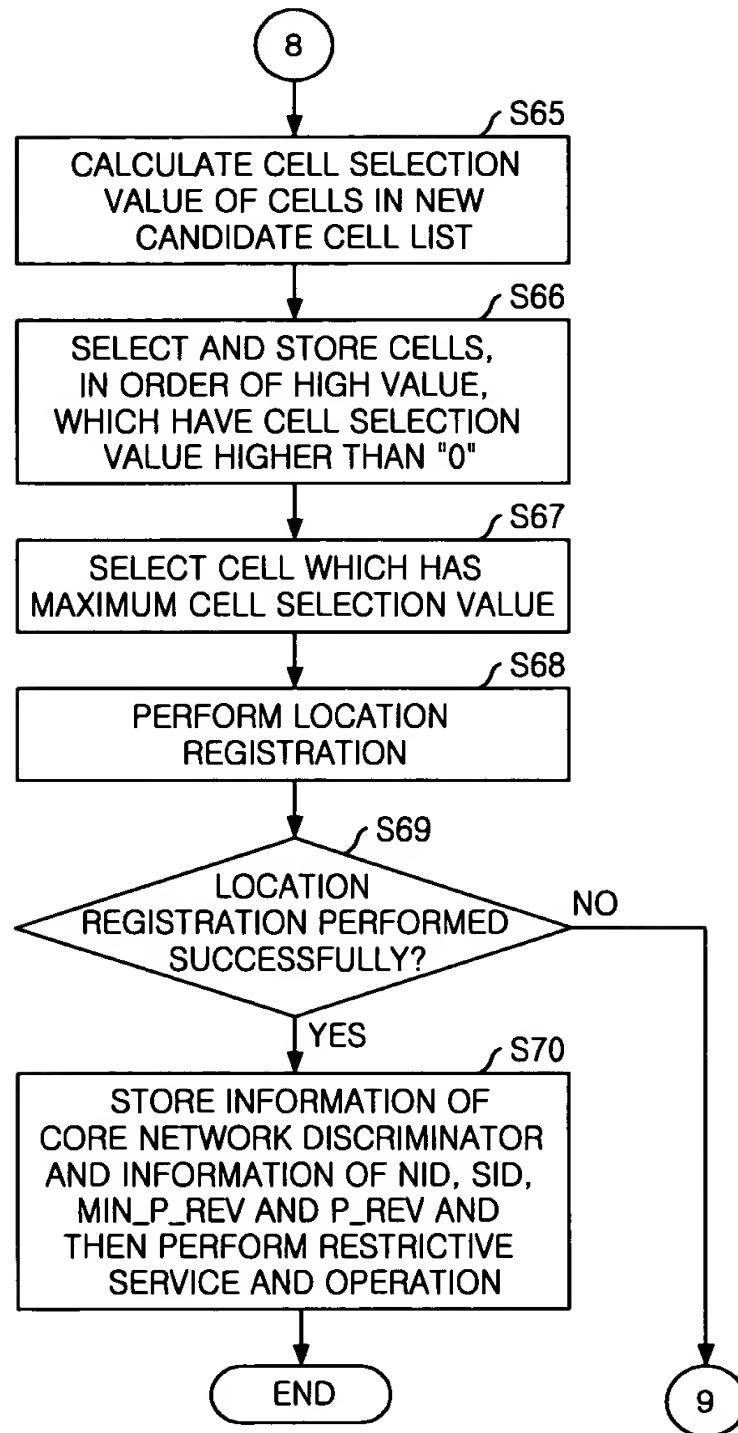


FIG. 5H



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FIG. 5I

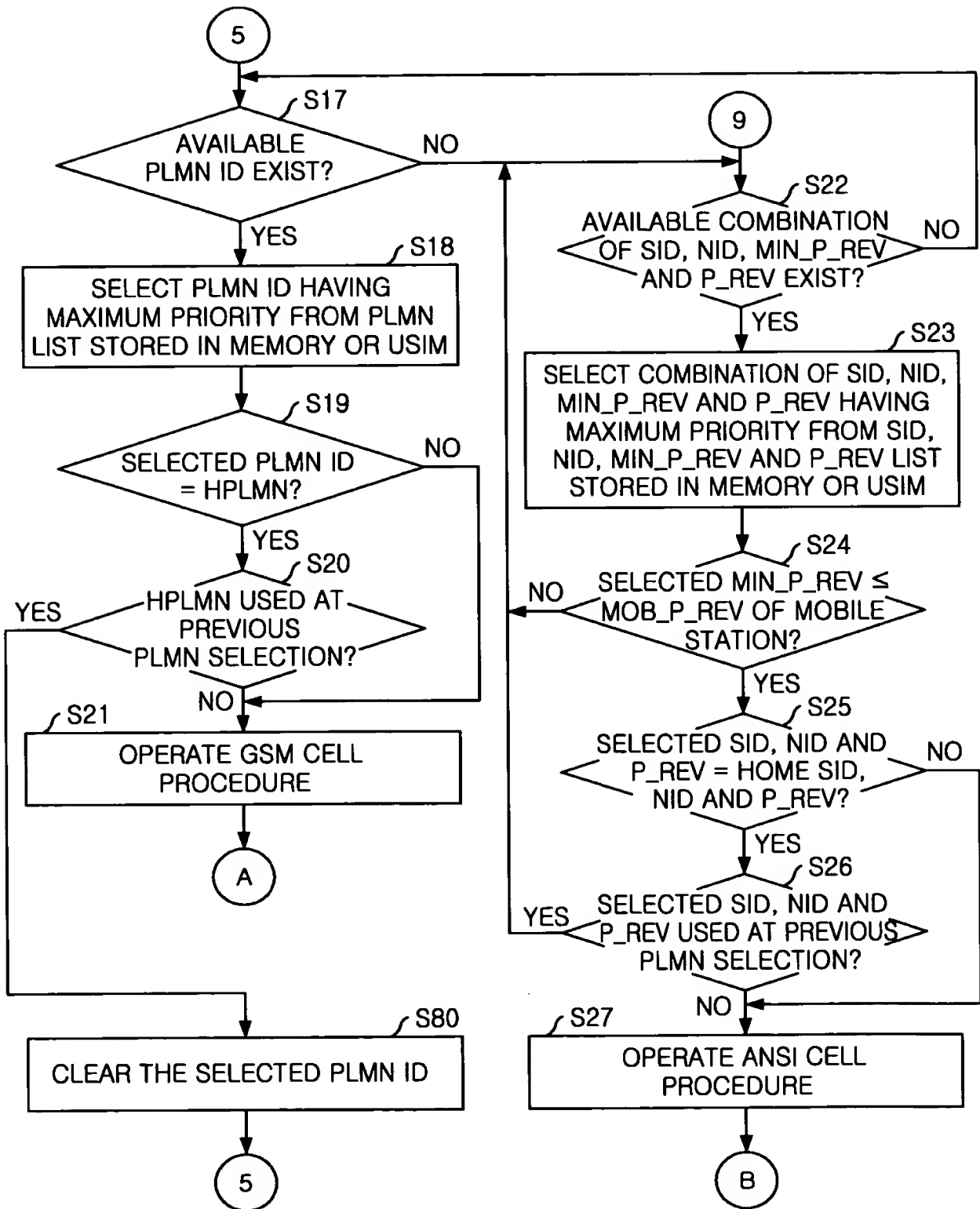


FIG. 5J

